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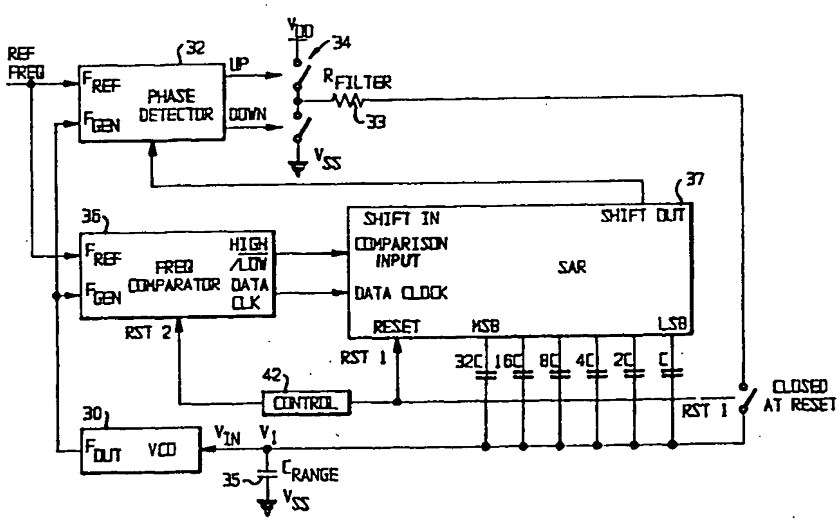

(57) Abstract

A local generated frequency is brought inot synchronization with a reference frequency using a phase-locked loop (PLL) which is configured to operate in a way to reduce the lock time required to achieve synchronization. The PLL includes a voltage-controlled oscillator (VCO) for generating the local frequency in response to an adjustable input control voltage to the VCO, and a phase detector for adjusting the control voltage according to a lack of synchronization between the local frequency and the reference frequency. Initially, a successive approximation process is performed to rapidly adjust the control voltage applied to the VCO in a direction to reduce the frequency offset of the local frequency from the reference frequency and thereby rapidly move toward synchronization therebetween. The phase detector is then enabled to perform a final adjustment of the control voltage to complete the synchronization.

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PHASE-LOCKED LOOP WITH FAST LOCK AND LOW JITTER

Background of the Invention

The present invention relates generally to phase-locked loop circuits, and more particularly to improvements in starting up and stabilizing phase-locked loops.

Phase-locked loops (PLLs) are often used in integrated circuit (IC) devices to synthesize a fast (high frequency) clock based upon a slower clock. A suitable example of this need is in the presence of noise sensitive environments. Since most of the electrical noise of a system is generated by the off chip clock, it is advantageous to use a slower, low noise clock in the system and use a PLL to multiply the clock frequency inside the chip product.

In a classical implementation, a PLL circuit (**FIG. 1**) includes a phase detector **10** at the input side of the circuit to receive the reference clock signal and the local clock signal at inputs **11** and **12**, respectively. The phase detector compares the phases of the two signals and supplies either an "up" signal or a "down" signal as a digital control signal to a charge pump **13**, depending on whether the local clock signal is lagging or leading the reference clock signal, respectively. The charge pump **13** generates an analog version of the control signal at its output **14**, which is fed through a low-pass loop filter **15** to remove or substantially reduce the higher frequency components and clock jitter otherwise attributable to oscillation of the local clock about the lock point. The output of the loop filter **15** is applied as an analog control input to a voltage-controlled oscillator (VCO) **17**. If the control signal that derives from the phase

detector **10** is up, the output frequency of VCO **17** is iteratively increased by amounts ultimately sufficient to bring the phase-lagging local clock signal into alignment (synchronization) with the edge of the reference clock signal. On the other hand, if the control signal is down, the VCO output frequency is commensurately decreased to bring the phase-leading local clock signal back into alignment with the edge of the reference clock signal.

The time interval consumed for the PLL to lock in phase alignment onto the reference signal or other input signal is referred to as the "lock time" (or sometimes, as the "start time" or "start-up") of the PLL. In general, a considerable lock time -- delay -- is typically experienced with PLL circuits heretofore available. Indeed, it is not unusual for the lock time to run 60 to 70 milliseconds (msec) or more. And a slow lock time for a semiconductor PLL chip requires that the chip be held in reset during the lock time interval.

The typical prior art PLL is characterized by the two main control elements, namely, the VCO and a correction device such as the phase detector, in a feedback path. The correction factor provides a voltage adjustment for the VCO, according to whether the phase (or frequency) is too fast or too slow relative to a reference phase. A PLL with a highly stable output frequency usually has a very long lock time because the increment of correction is quite small; indeed, this is what tends to maintain device stability. On the other hand, generally if the circuit has a large increment of correction, the appropriate phase or frequency adjustment can be achieved very quickly, but with undesirable rapid jitter.

One prior art technique which has been advanced as a possible solution to the problem of substantial lock time is to use a lock detect bit, which effectively instructs that nothing is to be done until the detect bit goes active. But among other problems that arise from this technique is the inability to detect a proper lock, so this has not provided an adequate solution.

According to an invention disclosed in co-pending application Serial No. 08/779,907, filed January 7, 1997, in the names of Jennifer Chiao and Randy L. Yach, and commonly assigned herewith ("the '907 application"), the lock time interval of the PLL is reduced to a manageable level, on the order of microseconds (μsec) in contrast to the usual response in milliseconds. The rapid start-up is particularly desirable for PLL usage in a system that performs a control function, such as in a microcontroller unit or device. The PLL has a loop filter with a preset reference voltage to bias the filter toward an immediate pump up requirement to a level which may even slightly overshoot the reference voltage level as a threshold. The loop filter is followed by a VCO.

When the PLL is on, the circuit commences from a zero voltage, essentially ground level in the usual manner, but because the reference node used in the circuit is not maintained at ground level, but rather at the predetermined reference voltage threshold, the pump up takes place at a steep ramp toward the threshold level. The reference is tantamount to a dynamic ground which assures that the PLL will move toward a rapid lock, oscillating upwardly from the threshold level to a point of stabilization at the equalization voltage and frequency. Lock time is achieved on the

order of microseconds versus other PLL circuit lock times which are typically greater by some three orders of magnitude.

In essence, the invention of the '907 application provides rapid synchronization of a locally generated frequency with a reference frequency by applying the local frequency and the reference frequency to a phase comparator of the PLL to generate a control signal indicative of the need to pump up or to pump down the local frequency to phase lock it to the reference frequency, applying a signal voltage derived from the control signal to a VCO of the PLL to vary the local clock frequency as necessary for the phase locking, and adjusting the signal voltage before application to the VCO by delivering the control signal to a loop filter of the PLL to bias the control signal toward a preset reference voltage threshold level selected to reduce the time necessary to achieve the desired phase locking. The preset reference voltage threshold level is applied to a node within the loop filter which will produce a rapidly ramped, virtual step change of the control signal, and thereby, of the signal voltage applied to the VCO. The advantages of this PLL circuit are accomplished without the penalty of substantially increased processing costs or silicon real estate costs.

It is a primary objective of the present invention to provide a PLL circuit that achieves a fast lock with low jitter using a capacitive digital-to-analog converter (DAC) approach, in which the DAC provides a rapid gross adjustment or correction of the VCO frequency relative to a reference frequency, and the conventional phase detector provides a fine adjustment to reach the frequency match.

Another aim of the invention is to use a successive approximation approach for such a DAC.

Summary of the Invention

The present invention provides a very stable, single frequency PLL with extremely short lock time. The PLL circuit includes a VCO and a capacitive digital-to-analog converter (DAC). Pulse widths are measured between the VCO-generated frequency and a reference frequency. A correction factor is derived from a comparison of the VCO-generated frequency and the reference frequency, and is fed to the DAC so that upon start-up of the device the DAC does a successive approximation of the correct voltage to be applied to the VCO to produce the appropriate matching frequency of the reference frequency. That part of the PLL circuit provides a gross adjustment. In addition, the customary correction applied in existing PLL circuits by a phase detector is utilized to provide a fine adjustment upon completion of the steps of successive approximation. The gross-corrected control voltage for the VCO is held as the binary output of the successive approximation register, and the phase detector is used for fine adjustment by varying the status of the successive approximation register, as a final voltage correction factor to the VCO.

Brief Description of the Drawings

The above and still further aims, objects, aspects, features and attendant advantages of the present invention will become apparent from a consideration of the following detailed description of the best mode currently contemplated for practicing the invention, encompassed by certain preferred methods and embodiments, taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a classic implementation of a PLL system, described in the above background section;

FIG. 2 is a block diagram of a preferred embodiment of a PLL according to the present invention;

FIG. 3 is a timing diagram for the PLL of **FIG. 2**; and

FIG. 4 is a block diagram of an exemplary embodiment of a frequency comparator for the PLL of **FIG. 2**.

Detailed Description of the Preferred Methods and Embodiments

Referring to the block diagram of **FIG. 2**, which illustrates a phase-locked loop according to a preferred embodiment of the invention, the circuit includes voltage controlled oscillator (VCO) **30** and phase detector **32** which are typical components of a conventional PLL. In the circuit of the present invention, however, the phase detector is employed for fine adjustment or fine tuning of the final (match) frequency generated by VCO **30**. The VCO-generated frequency (or simply, the

generated frequency) F_{OUT} is applied as F_{GEN} to one input terminal of phase detector **32**. A reference frequency F_{REF} with which F_{GEN} is to be synchronized is applied as a second input to the phase detector. The phase detector develops an output in the form of an "up" signal or a "down" signal depending on whether the generator frequency is lagging or leading the reference frequency.

The specific output developed by phase detector **32** is a voltage level between the supply voltage V_{DD} for the semiconductor circuit chip on which the PLL circuit is fabricated (which may be integrated, for example, with a microcontroller or MCU (not shown) to be used for controlling a parameter of a system of a type that depends on the specific application in which the MCU is used) and the circuit ground V_{SS}. The phase detector output voltage develops a current through and voltage drop across a filter resistor **33**, resulting in an adjustment, up or down as the case may be, to a voltage V1 which is applied as a control voltage to the V_{IN} input of VCO **30**. A static capacitor **35** is connected between V1 and V_{SS} to be charged up and to limit the voltage range to the VCO.

Thus, if F_{GEN} is lagging F_{REF}, phase detector **32** will generate an "up" voltage which adjusts the voltage V1 applied to the VCO **30** to increase the output frequency F_{GEN} of the latter (decrease its period) to move it toward (and ultimately into) synchronization with F_{REF}. On the other hand, if F_{GEN} is leading F_{REF}, a "down" voltage is developed by the phase detector and voltage V1 is fined tuned downward to decrease the frequency of the VCO (increase its period) toward (and ultimately into) synchronization with F_{REF}.

The phase detector relies on clock pulse edges. For example, the detector may observe that the reference clock edges are arriving sooner than the generator clock edges, which necessitates that the generator frequency must be increased. This causes the "up" output of the phase detector to close an associated switch **34** momentarily to raise the voltage on the filter resistor **33**, and charge up capacitor **35**, thereby increasing the voltage V1 at the input V_{IN} of VCO **30**, and the frequency generated at the output of the VCO. The value of filter resistor **33** is chosen to be sufficiently large that small differences in phase will not produce large changes in the input voltage to the VCO, to avoid the possibility of fluctuation about the correct frequency. On the other hand, the filter resistor value should not be so large that an inordinate amount of time is required for the node on the opposite side of the resistor to reach the voltage appropriate to achieve a match of the reference frequency.

Phase detector **32** and VCO **30** may of completely conventional implementation to perform their respective functions. If the phase-locked loop of **FIG. 2** consisted solely or essentially of the VCO and the phase detector and their associated components discussed thus far, the lock time would be unacceptably long for most applications, where low jitter is paramount. Likewise, a short lock time would be accompanied by substantial jitter.

According to the invention, a gross adjustment of the VCO-generated frequency is made first, before the fine adjustment performed by the phase detector in concert with the VCO, toward fast locking of the PLL to the correct frequency, i.e., an F_{GEN} that matches F_{REF}, with low jitter. To that end, a particular type of digital-to-

analog converter (DAC) is incorporated in a loop which is separate from the loop containing the phase detector in the PLL but part of the input filter to the VCO voltage input. In essence, the DAC is used to provide a rough but extremely fast correction of F_{GEN}, and then the phase detector completes the final adjustment for correction to produce a match of F_{REF}.

The DAC includes frequency comparator **36** and successive approximation register (SAR) **37**. Initially, the SAR estimates (i.e., is preset such that) the voltage value it must generate should produce a frequency at exactly the midpoint of the frequency range of the VCO. The frequency comparator then compares the frequency F_{GEN} generated by VCO **30** to the reference frequency F_{REF}, much as the phase detector **32** compares the phases of the two. In this instance, however, the purpose is to produce an absolute data value (high or low) based on whether the comparison finds that the generator frequency is higher or lower than the reference frequency, respectively. This data value from the frequency comparator is then applied to SAR **37**. In response, the SAR generates a new step voltage to be applied to the VCO, and the cycle repeats itself. The objective is to cause the SAR to rapidly generate an output voltage V1 that will result in the VCO quickly attaining an output frequency F_{GEN} that matches the reference frequency, in relatively few successive approximation steps.

This objective is achieved by causing the SAR to estimate the final value of voltage V1 for the matching generator frequency, by successively dividing the voltage range for V1 in half, and thereby, the frequency range to be generated by the

VCO, with the only decision being whether the correct value lies in the upper or the lower half of each successive range. It will be appreciated that this successive halving of the control voltage in steps will, with selection of the appropriate half of the then existing range each time, result in rapid attainment of the correct VCO input voltage V_{IN} and, thus, the correct VCO output frequency F_{GEN}. Final adjustment of the input voltage to arrive at the correct frequency is commenced and completed through the phase detector loop when the SAR (and the overall DAC) has completed its gross adjustment cycle.

The exemplary 6-bit SAR **37** (which may of a greater or lesser number of bits, if desired) is generally of conventional implementation except that its output is taken across a plurality of capacitors **40** connected in parallel, each constituting a respective bit value ranging from a most significant bit (MSB) to a least significant bit (LSB) in steps of **32C**, **16C**, **8C**, **4C**, **2C**, and **C**, respectively. Binary bits drive the capacitors from the MSB down to the LSB, the MSB driving a 32 unit capacitor (**32C**), the next MSB driving a 16 unit capacitor **16C**, and so forth through 8, 4, 2, and down to the LSB which drives the single unit capacitor **C**. In this way, the largest approximation step is created for the MSB, which estimates a voltage (and a frequency) at one-half -- the midpoint of the respective range, then one-quarter (relative to the overall range), one-eighth, and so forth, in binary weighted fashion.

The timing diagram of **FIG. 3** illustrates this operation, each part of the Figure indicating the situation at a different point in the circuit. Part **A** shows the application of a reset 1 (RST1) to SAR **37** and to trigger the closure of a switch **41**

according to the minimum input voltage for the VCO. Part **B** indicates the timing for reset 2 (RST2), which is applied to frequency comparator **36**. Each of the resets is produced by a control unit **42**. The control unit is conventional logic circuitry whose primary function is to hold the gross system in reset until the VCO is stable following each frequency change (or initiation). If the system were allowed to operate before the VCO attained a stable frequency, the DAC would simply vacillate and thereby unduly lengthen the lock time. Control unit **42** also holds the phase detector **32** in reset mode until the gross system is out of reset, controls the overall timing, enables a check of the frequency comparator output at the SAR after reset is released, and initiates the SAR movement through its stepping function (part **C** illustrating the timing for SAR out). For each step the frequency comparator is again held in reset until the VCO has had sufficient time to stabilize (part **D** of **FIG. 3** showing the timing for the frequency comparator data (high/low) out). This cycle continues until the SAR stepping is completed.

SAR **37** comprises a conventional shift register (not shown), which at the last stage produces a shift out as a binary 1 (part **E** of **FIG. 3**) to enable phase detector **32** to commence fine adjustment of the VCO to the correct frequency and, in the interim, to temporarily disable (i.e., suspend operation of) the frequency comparator and the SAR for the sake of power conservation after the gross margin has been completed and during operation of the phase detector for fine tuning the final frequency.

Part **F** of the timing diagram of **FIG. 3** illustrates the stepped excursion of voltage V1 through the operation of the frequency comparator and the SAR. V1 -- the voltage input to the VCO -- ranges between minimum and maximum values, for which the SAR selects the midpoint in the beginning step. The frequency comparator **36** then compares the resulting generator frequency against the reference frequency and makes a decision whether this F_{GEN} is high or low by which to select the appropriate portion of the range to be addressed for the next step or iteration, and so forth until the gross adjustment cycle is completed. Although part **F** shows solid line branching of the voltage V1, the selection process will result in only one path along the successive iterations of the gross adjustment through the SAR LSB, at which time the phase detector takes over to complete the task to arrive at a final value of V1 (and F_{GEN}). This enables the overall PLL to rapidly reach the correct (i.e., the matching) frequency, so that when the frequency comparator and SAR are used, together with the phase detector, only a relatively few clock cycles are required for the VCO to attain the correct frequency.

In the exemplary embodiment of **FIG. 4**, frequency comparator **36** comprises a pair of n-bit (where n is the minimum size) racing counters **50** and **51**, the former for the generator frequency F_{GEN}, and the latter for the reference frequency F_{REF}. In this example, each is a 3-bit counter. The reset for each counter is released simultaneously so that both counters commence running at the same time, and the MSB value that comes up first wins the race. It should be noted that when the MSB is set, it can only be cleared by a control reset (RST2). Assume, for example, that the generator

frequency clocks faster than the reference frequency. In that instance, the counter **50** MSB will go to a 1 first, before the MSB of counter **51** goes high. Consequently, a 1 is applied to the D input of a flip-flop (bistable multivibrator) **52** before counter **51** can generate a clock input to that flip-flop. Flip-flop **52** then clocks out a 1 as the data value to indicate that the generator frequency is higher than the reference frequency.

Conversely, where the generator frequency is slower than the reference frequency, the MSB of counter **50** will be a 0 at the time when the MSB of counter **51** goes high. In that case, a 0 is applied to the D input of flip-flop **52** at the rising edge of the reference MSB, and a 0 is then clocked from the output of the flip-flop as the data value to indicate that the generator frequency is too slow, and that the SAR must increase the frequency by moving to the midpoint of the next proper range.

The delay path is determined by the number of bits in each n-bit counter. Accordingly, n should be selected as a compromise or trade-off between relatively good resolution of which of the two clocks (frequencies) is the faster (or the slower) and the period of time in which that determination should be made. Selection of $n = 1$ is a poor choice because it would result in a constant race of clock pulse rise times, but $n = 8$ is also a poor choice because it necessitates a rather long wait to determine which clock is the faster. A 3-bit counter is preferred as the minimum count to determine clock speed. This requires a count of 4 -- from 0 to 3 -- each time the MSB (or successive bit of those from the SAR) goes to a 1, and the SAR must go through 6 steps (in the exemplary embodiment of **FIG. 2**), so the loop must go through $4 \times 6 = 24$ clock cycles to arrive at the gross adjustment in this example.

In addition, some "overhead" must be taken into account because each time the input voltage to the VCO is stepped to a new level, some time interval must elapse before the VCO stabilizes at the new frequency. Otherwise, as noted earlier herein the frequency comparator will chase a moving frequency, with resulting inaccuracy. The reference frequency and the reference counter **51** together with associated flip-flops **54** and **55** also provide the data clock to the SAR, to indicate the presence of valid data to be clocked into the SAR, for shifting in the proper bits.

In an optimum system, the VCO output will include a divide-down circuit in recognition that the reference frequency is generally a low frequency input, e.g., 32 Khz, and the desired generator frequency is a multiple of that, e.g., $F_{GEN} = 16 \times F_{REF}$. In that example, a divide-by-16 counter (not shown) would be coupled to the F_{OUT} output of VCO **30**, to bring the generator frequency to the desired value, in effect multiplying 32 Khz by 16.

A capacitive DAC is preferred over any other type of DAC approach or other type of gross adjustment system. If a 1 were entered as the MSB and a 0 for each of the other bits, the first capacitor **32C** is charged up while the others are held uncharged, so that a capacitive division exists between that capacitor and all of the others. By weighting all of the capacitors, a resulting value is derived which constitutes the DAC value. If all of the SAR capacitors were at 0, the node for the first capacitor may still be charged to a starting value which represents the minimum of the VCO input range for the lowest frequency by inserting capacitor **35** as a range limiter to prevent the node at which V1 appears to go all the way from circuit ground V_{SS} to the

chip supply voltage V_{DD}. This assures that when the VCO commences from the minimum voltage level, successive divisions will be performed at half the VCO range.

Importantly, because the SAR performs together with the comparator as a capacitive DAC, when the SAR stepping is completed, the phase detector can effect a change in the capacitive voltage, if necessary for the fine tuning to the correct VCO frequency. The binary value of the SAR is maintained, and the V1 node can be charged or discharged as desired because it appears to be a capacitive load to the phase detector. If a resistive DAC were used, the phase detector would be unable to make a change in the voltage (or the frequency) because its output would be held resistively at a final value. Thus, a resistive ladder could not be substituted for the capacitive array. Similarly, a slope converter would not suffice because it is tends to ramp up slowly from a minimum value to a target value.

Although a best mode currently contemplated for practicing the invention has been described herein, in conjunction with certain preferred methods and embodiments, it will be recognized by those skilled in the art of the invention that variations and modifications of the disclosed methods and embodiments may be made without departing from the true spirit and scope of the invention. Accordingly, it is intended that the invention shall be limited only by the appended claims and the rules and principles of the applicable law.

Claims

1. A method of synchronizing a local generated frequency with a reference frequency using a phase-locked loop (PLL) having a voltage-controlled oscillator (VCO) to generate the local frequency in response to an adjustable input control voltage to the VCO and a phase detector to adjust the control voltage according to a lack of synchronization between the local frequency and the reference frequency, the method comprising the steps of applying the local frequency and the reference frequency to a capacitive digital-to-analog converter (DAC) to develop a gross adjustment of the control voltage to be applied to the VCO for rapid correction of the synchronization therebetween before the phase detector is permitted to adjust the control voltage therefor, and responding to completion of the gross adjustment by enabling the phase detector to further adjust the control voltage for final correction of the synchronization, whereby to reduce the lock time of the PLL.

2. The method of claim 1, wherein the step of applying the local frequency and the reference frequency to the capacitive DAC to develop a gross adjustment of the control voltage includes comparing the local frequency and the reference frequency to determine which of the two is the higher, and using the determination to perform a binary-weighted successive approximation of the adjustment required to be made to the control voltage as a gross correction thereof for application to the VCO.

3. The method of claim 2, wherein the binary-weighted successive approximation is performed by applying a succession of bits of selected value from a most significant bit to a least significant bit to a plurality of parallel-connected capacitors equal in number to the number of said bits from most to least significant, for charging said capacitors to provide a gross correction of the control voltage.

4. The method of claim 3, wherein the respective values of said succession of bits are selected to successively halve the range of the control voltage between a predetermined minimum voltage and a predetermined maximum voltage.

5. The method of claim 3, wherein the further adjusting of the control voltage with the phase detector includes presenting said plurality of capacitors as a capacitive load for charging or discharging thereof by the phase detector.

6. Phase-locked loop (PLL) apparatus for synchronizing a locally generated frequency with a reference frequency, wherein said PLL apparatus includes a voltage-controlled oscillator (VCO) for generating the local frequency in response to an adjustable input control voltage thereto, and a phase detector responsive to both the local frequency and the reference frequency for adjusting the control voltage according to a lack of synchronization therebetween for control of the VCO toward synchronization thereof, said PLL apparatus further comprising a capacitive digital-to-analog converter (DAC) for gross adjustment of the control voltage to effect a rapid synchronization between the local frequency and the reference frequency before fine adjustment of the control voltage by the phase detector, means for applying the local frequency and the reference frequency to said DAC, and means for enabling the phase

detector to perform said fine adjustment in response to completion of the gross adjustment, whereby to reduce the lock time of the PLL.

7. The PLL apparatus of claim 6, wherein the DAC includes means for performing a binary-weighted successive approximation of the adjustment required to be made to the control voltage as a gross correction thereof for application to the VCO.

8. The PLL apparatus of claim 7, wherein said successive approximation means includes a plurality of parallel-connected capacitors and means for applying a succession of bits of selected value from a most significant bit to a least significant bit to said plurality of capacitors for charging thereof to provide a gross correction of the control voltage, said capacitors being equal in number to the number of said bits from most to least significant.

9. The PLL apparatus of claim 7, wherein said successive approximation means includes means for successively halving a range of the control voltage between a predetermined minimum voltage and a predetermined maximum voltage, to speed arrival at said gross adjustment for application to the VCO.

10. The PLL apparatus of claim 7, further including means for coupling said plurality of capacitors as a capacitive load to the phase detector for charging or discharging thereof by the phase detector to effect said fine adjustment of the control voltage.

11. Phase-locked loop (PLL) apparatus for synchronizing a generated frequency with a reference frequency, the PLL apparatus including a voltage-

controlled oscillator (VCO) responsive to an adjustable input control voltage to produce said generated frequency, and a phase detector responsive to a lack of synchronization between said generated frequency and said reference frequency to adjust the control voltage for control of the VCO to achieve said synchronization, the PLL apparatus further comprising successive approximation means for rapidly adjusting the control voltage toward synchronization between the generated frequency and the reference frequency before said adjustment of the control voltage by the phase detector, means for applying the generated frequency and the reference frequency to said successive approximation means, and means for enabling the phase detector to complete said adjustment for final synchronization between said generated frequency and said reference frequency, whereby to reduce the lock time of the PLL.

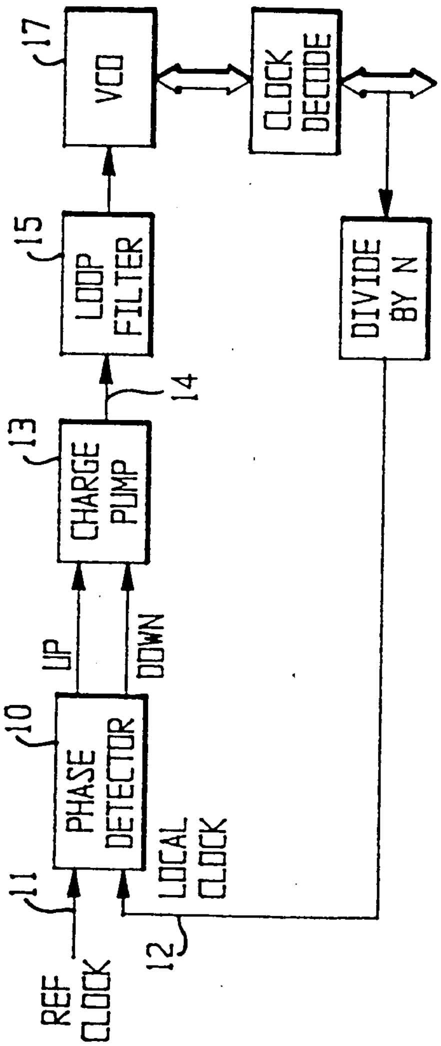
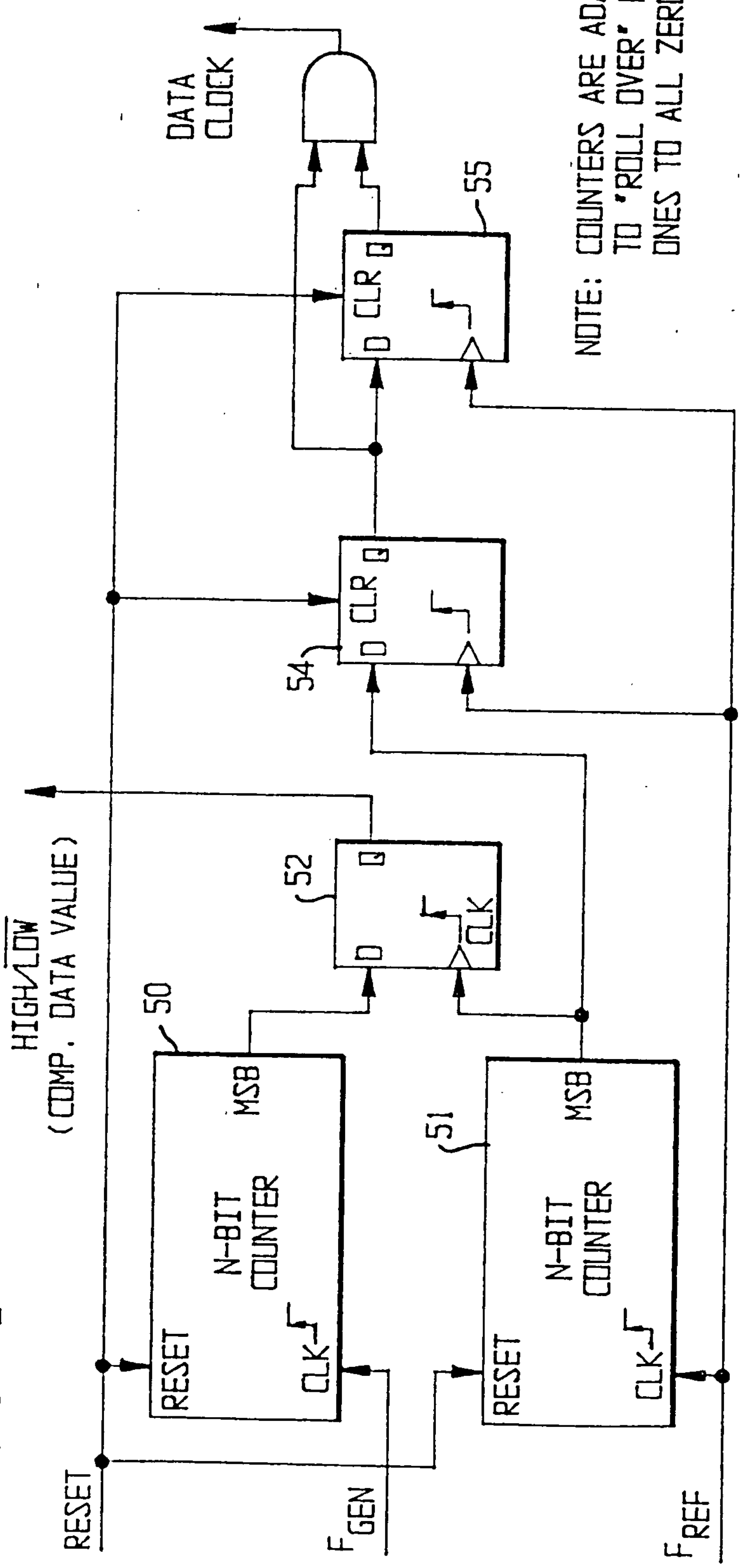
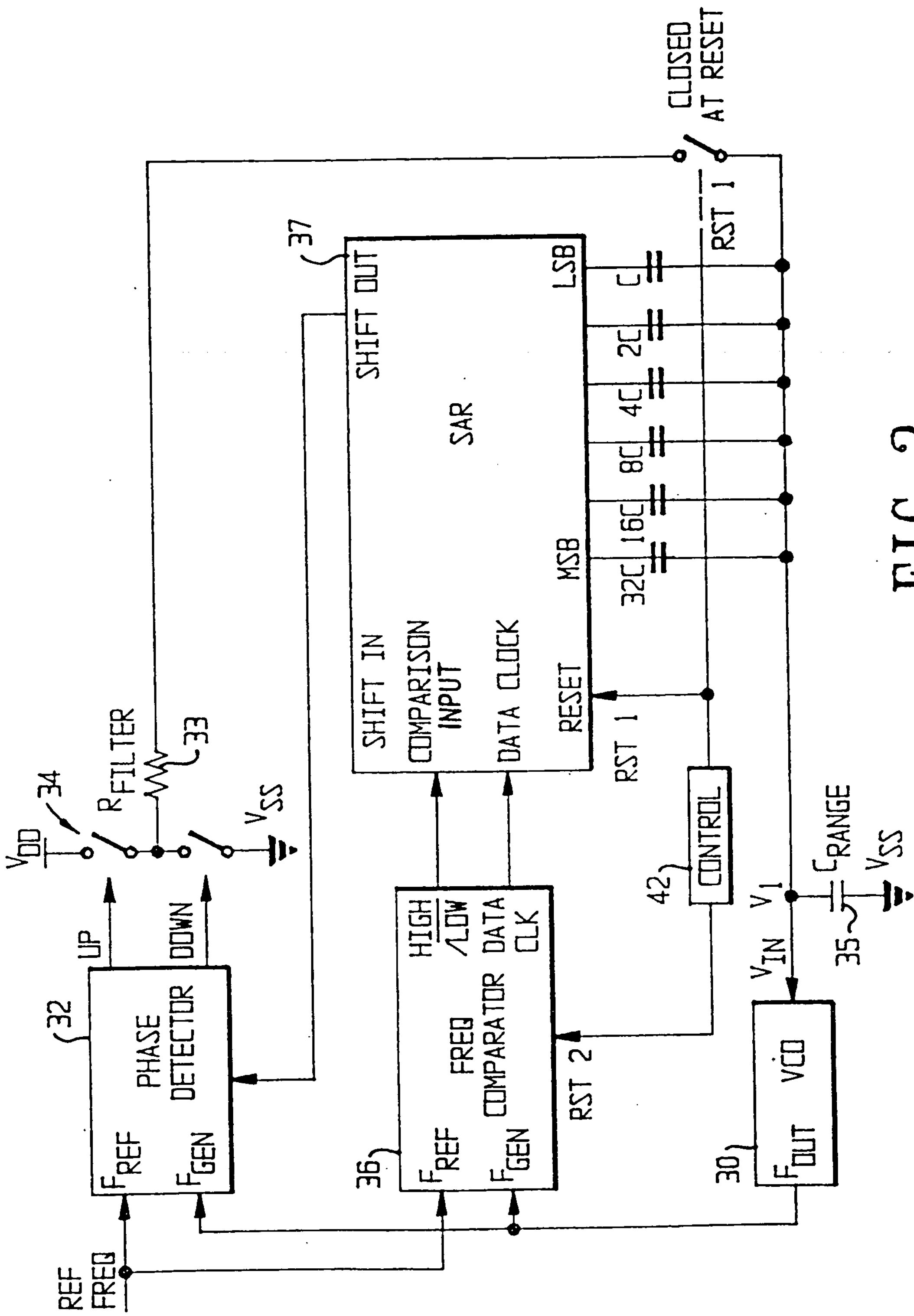


FIG. 1
(PRIOR ART)



NOTE: COUNTERS ARE ADAPTED NOT TO "ROLL OVER" FROM ALL ONES TO ALL ZEROS.

FIG. 4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INPUT
DATA CLOCK
RESET
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CONTROL
42
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CRANGE
VSS
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VIN
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30
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32
PHASE
DETECTOR
FREF
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COMPARATOR
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36
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FREQ

FIG. 2

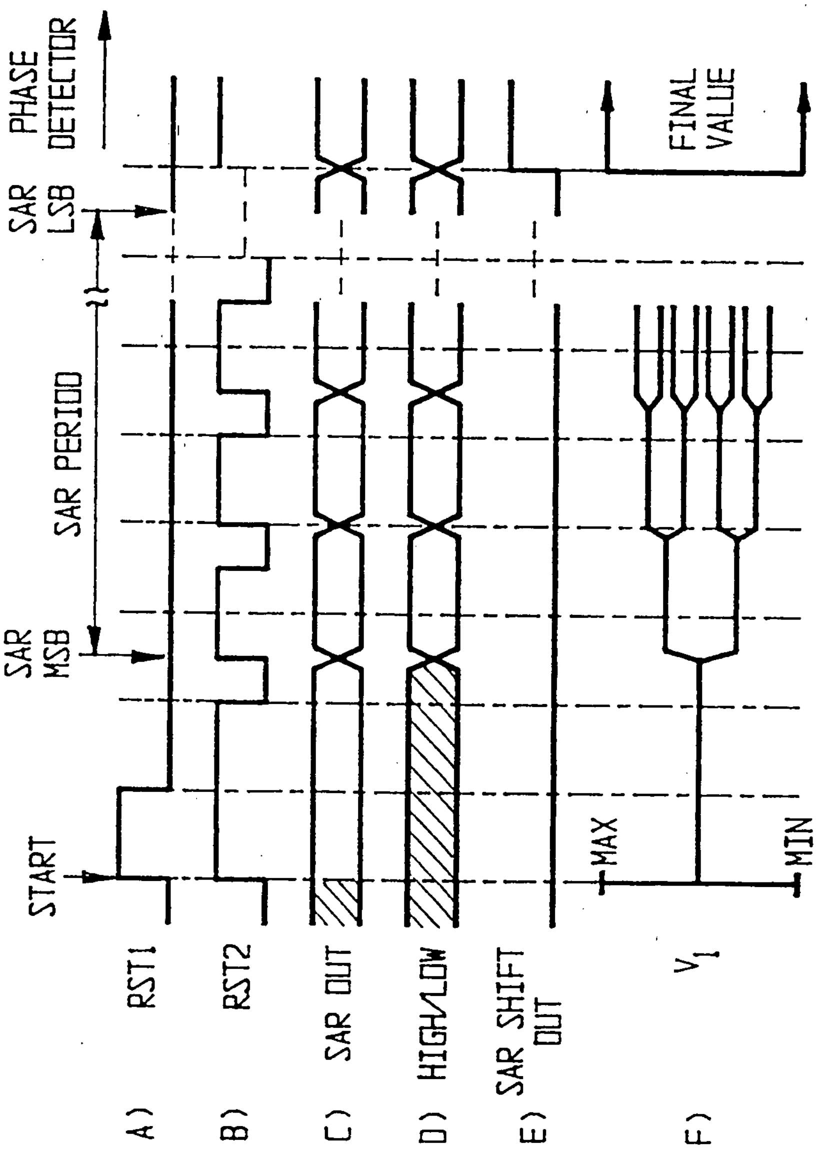
A) RST1
B) RST2
C) SAR OUT
D) HIGH/LOW
E) SAR SHIFT OUT
F) V_1
START
SAR MSB
SAR PERIOD
SAR LSB
PHASE DETECTOR
MAX
MIN
FINAL VALUE

FIG.3

INTERNATIONAL SEARCH REPORT

Interna[illegible]l Application No
PCT/US 98/14785

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03L7/113

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 94 26041 A (RCA THOMSON) 10 November 1994 see page 4, line 13 - page 6, line 33 see page 7, line 29 - page 9, line 20 see page 12, line 1 - page 13, line 10 see page 14, line 25 - line 30 see page 16, line 8 - page 17, line 32 see page 19, line 7 - line 27; figures 1,2A,2B,5,6 ---	1-11
A	GB 2 305 558 A (FUJITSU LTD.) 9 April 1997 see page 15, line 7 - page 25, line 2; figures 1-3 --- -/--	1-11

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
8 October 1998	19/10/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Butler, N

1

Internal Application No
PCT/US 98/14785

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 281 927 A (L. PARKER) 25 January 1994 see column 3, line 4 - column 4, line 3; figure 1 see column 6, line 13 - line 63 see column 8, line 51 - column 10, line 10; figures 4,5; table 1 ---	1-11
A	EP 0 768 756 A (PIONEER ELECTRONIC CORP.) 16 April 1997 see column 3, line 53 - column 4, line 25 see column 17, line 46 - column 21, line 52; figures 8,11,16,20 -----	1-11

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Internat Application No
PCT/US 98/14785

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 98/14785

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